## REMARKS

This paper is filed in response to the office action mailed on February 24, 2005.

In the office action, the Information Disclosure Statement filed on March 19, 2004 is objected to as copies of the non-patent literature publications were not provided with the statement. A Supplemental Information Disclosure Statement including those items is submitted herewith.

The office action also objects to Fig. 1 as filed. In response, an amended Fig. 1 is submitted herewith.

The office action also objects to the abstract. In response, an amended abstract is submitted herewith.

Finally, the office action also objects to paragraph 0015 of the application as filed. In response, paragraph 0015 is amended to traverse this objection.

The office action also makes numerous objections to the claims are filed. However, claims 1-24 have been canceled in favor of new claims 25-31. In the drafting of new claims 25-31, the examiner's objections have been kept in mind and applicant appreciates the examiner's careful review of claims 1-24.

Turning to the rejections based upon the prior art, original claims 1 and 22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,304,978 ("Horigan"). In response, claims 1-24 have been canceled and new independent claims 25 and 29 are presented herewith.

Applicant respectfully submits that Horigan cannot serve as an anticipating reference under MPEP § 2131 because Horigan does not teach or suggest a separate system to which a current signal is transmitted and which has a memory that includes a utilization utility for determining a percentage utilization. Horigan also fails to teach a target memory in which a maximum current utility is stored. Horigan also does not teach or suggest a system for optimizing utilization and dealing with processor bottlenecks by increasing current consumption by the target processor as recited in claim 25 or the method for dealing with processor bottlenecks recited in independent claim 29.

Therefore, the anticipation rejections based upon Horigan are rendered moot in view of the presentation of new claims 25-31.

Next, the office action rejects claims 1-8 and 22-24 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 6,721,672 ("Spitaels"). In response, claims 1-24 have been canceled in favor of new claims 25-31.

Spitaels, also fails to teach or suggest any method for dealing with processor bottlenecks and therefore cannot serve as an anticipating reference under §2131 either. Spitaels only keeps track of the maximum current usage for a processor to detect "potential overload condition[s]" (column 8, line 31) or to draw maximum current values (column 9, lines 42-56). Spitaels does not teach or suggest the comparing functions of independent claims 25 and 29 which are used to identify peak usage periods or bottleneck periods for a processor carrying out an application program and Spitaels in no way teaches or suggests increasing the amount of current being used by the target processor during these peak periods to increase processing speeds at the peak current usage times. Therefore, Spitaels teaches nothing about addressing the problems of processor bottleneck during the execution of a software application.

Therefore, in view of the presentation of new independent claims 25 and 29, applicant respectfully submits that the anticipation rejections based upon Spitaels are now moot.

Next, the Patent Office rejects claims 2-8, 23 and 24 under 35 U.S.C. § 103 as being unpatentable over Horigan in view of Spitaels. However, this rejection is rendered moot in view of the presentation of new independent claims 25 and 29.

Specifically, under MPEP § 2142,

> [t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

*Citing, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); *see also* MPEP § 2143-§ 2143.03 for decisions pertinent to each of these criteria.

No combination of Horigan and Spitaels teaches or suggests every claim element of independent claims 25 and 31 and therefore this obviousness rejection is improper. As noted above, Horigan fails to teach or suggest a separate system for evaluating the current being drawn by a target processor. The Horigan processor 205 in Fig. 2 or 405 in Fig. 4 is directly connected to a power supply 245 or 420. The throttle lines 262 or 407 are directly connected to their respective power supplies 240 or 420. Thus, there is no linking between a power line that connects a power supply and a target processor and a host system as illustrated in Fig. 1 of the present application and as recited in independent claims 25 and 29. Claim 25 recites that the sensor is linked to the host memory; claim 29 recites that a signal indicative of the amount of current being sensed is transmitted to the host system.

Spitaels also fails to teach or suggest the sensing of current being transmitted through a power line extending between a power supply and a target processor and transmitting a signal indicative of that current to a separate host system. Spitaels only teaches the use of a power control module 212 contained within a second computer 210 as shown in Fig. 2. However, the computer 210 is not linked to any power supply line as illustrated in Fig. 1 of the present application and recited in claims 25 and 29.

Spitaels does teach the monitoring of current levels for the possibility of potential overload conditions (column 8, line 31) and the increasing of power draw to a maximum as explained in column 6. However, independent claims 25 and 29 clearly go a step further by determining percentage utilizations with the utilization utility recited in claim 25 and using the maximum current utility to increase amounts of current used by the target processor during peak usage time to alleviate bottleneck conditions. Independent claim 29 recites equivalent process steps. Spitaels does not teach or suggest any means for identifying peak usage times and increasing current to the target processor to alleviate bottleneck problems.

Therefore, no hypothetical combination of Horigan and Spitaels teaches or suggests every element of independent claims 25 and 29 and therefore the obviousness rejection based upon these two references is moot.

Next, the office action rejects claim 9-16 and 18-21 under 35 U.S.C. § 103 as being unpatentable over Spitaels in view of U.S. Patent No. 6,057,839 ("Advani").

The deficiencies of Spitaels are discussed above. Advani is cited for the proposition that is teaches the graphical display of processor activity. However, the graphical

displays of Advani are not based upon current usage and Advani does not teach or suggest the tapping of a power line to monitor current usage by a processor and sending a signal indicative of the current usage to a separate host system. Therefore, Advani cannot supplement the deficiencies of Spitaels and accordingly no hypothetical combination of Spitaels and Advani teaches or suggests every element of independent claims 25 and 29.

Finally, the office action rejects claim 17 under 35 U.S.C. § 103 as being unpatentable over Spitaels, Advani and further in view of U.S. Patent No. 4,823,075 ("Alley"). The deficiencies of Spitaels and Advani are discussed above. Alley is only cited for the proposition that it teaches the use of a Hall-effect sensor. Alley is not cited for the proposition that it teaches any means for monitoring current usage of a target processor and increasing current usage during peak usage time to alleviate bottleneck problems. Therefore, Alley cannot be used to supplement the deficiencies of Spitaels and Advani to establish a *prima facie* case of obviousness. Accordingly, in view of the cancellation of claim 17 and the presentation of new claims 25 and 29, applicant respectfully submits that the obviousness rejection based upon Spitaels, Advani and Alley is now moot.

An early action indicating the allowability of this application is respectfully requested.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855.

Dated: May 24, 2005

Respectfully submitted,

By_____
Michael R. Hull
Registration No.: 35,902
MARSHALL, GERSTEIN & BORUN LLP
233 S. Wacker Drive, Suite 6300
Sears Tower
Chicago, Illinois 60606-6357
(312) 474-6300
Attorney for Applicant

Attachment